REMARKS

Claims 1-15 are pending in the application. Claims 1 and 10 are independent. Claims 1, 4, 5, 7-10, 13 and 14 stand rejected. Claims 2, 3, 6, 11, 12, and 15 are objected to but would be allowable if rewritten in independent for.

Claims 1, 4, 5, 7-10, 13 and 14 stand rejected under 35 U.S.C. §102(b) as anticipated by Wynn et al. The Examiner has kindly pointed out where the Wynn reference supposedly illustrates the elements of the rejected claim.

Referring first to claim 1, the Examiner states that the "two bus users" in claim 1 are shown as the "fiber optic media and Ethernet links" in Fig. 1 of Wynn. It is respectfully submitted that these items might be considered buses but they are not bus users as that term is generally understood in the art. A bus is generally considered to be a data path (e.g. media or link) over which devices (bus users) communicate. The Examiner's interpretation of the phrase "bus user" seems to ignore the word user.

Next, the Examiner equates the "data bus" in claim 1 with the OTM 102 in Fig. 1 of Wynn. According to Wynn, the "OTM (optical termination module) 102 and STSMs (SONET STS-1 modules) 103 are termination modules of a public switched network transported by fiber optic media. OTM 102 and STSMs 103 convert and de-multiplex the OC-3 signals into DS0 channels for processing within delivery unit 10 and transport to switching system 11." Col. 5, line 66 et seq. This is hardly the equivalent of a data bus. It

is more closely related to a bus user. A data bus does not multiplex or demultiplex, it simply conveys data.

Turning now to the third element of claim 1, the clock bus, the Examiner refers to the STGS 115 in Fig. 1 of Wynn. Wynn describes this as the system timing generator. "STGS 115 generates timing signals from which delivery unit 10 and switching system 11 derive their timing. STGS 115 selects between one or more reference signals received for synchronizing its generated timing signals in accordance with SONET specifications. These reference signals may be provided by signals generated external to switching system 11 and delivery unit 10 or the may be derived from the OC-3 network signals terminated at delivery unit 10. STGS 115 also filters the timing signal to provide a high quality timing signal out." Col. 7, line 38 et seq. The STGS thus may be considered analogous to a clock source, but it is not a bus. Compare reference numerals 14 and 20 in the instant specification. The clock bus does not generate clock signals, it transports them. It is the clock source which generates the timing signals. It should therefore be clear that the STGS in Wynn does not read on the claimed clock bus. In fact, in Fig. 2 Wynn shows a "timing bus" which is indirectly coupled to the STGS.

The fourth element of claim 1 is the control line which the Examiner compares to the BCM 101 in Fig. 1 of Wynn. Clearly, the BCM is not a "line". It is a device which is coupled to many lines (they are shown as arrows). The Examiner has apparently confused media and devices in his analysis of claim 1 and has cited media as reading on devices and devices as reading on media.

Finally, the wherein clause requires that the control line be asserted when valid data from one of said asynchronous data streams appears in a slot of said repeating bus frame. In addressing this limitation of claim 1, the Examiner refers to col. 9, line 12 and col. 34, lines 31-43. These portions of Wynn refer to the SONET overhead fields, the MUX/DEMUX 291 and the path terminators 301-309. While the overhead fields of a SONET signal include an in-band control signal, such a signal does not amount to a control line as claimed and would not permit the function accomplished by the claimed invention. In Wynn, no mention is made of a control line being asserted or of anything being asserted. The only mention of control lines in Wynn is in reference to Fig. 19C which shows an interface between a PCI bus and a SCSI bus. The only mention of asserting lines in Wynn is in reference to Fig. 19 which concerns arbitrated requests and grants on a PCI bus.

For the foregoing reasons Wynn cannot possibly anticipate claim 1. Moreover, Wynn does not even suggest claim 1. Claims 4, 5, and 7-9 depend from claim 1 and thus the remarks made above apply to these claims as well.

Independent claim 10 is a method claim containing four steps. The last step is "asserting a first control line when valid data from one of the asynchronous data streams appears in a slot of the repeating bus frame" which corresponds to the wherein clause in claim 1. In rejecting claim 10, the Examiner states that the data streams in Wynn contain a start-of-frame bit as described at col. 26, lines 12-25. The Examiner does not explain how transmitting a bit in a data frame anticipates asserting a control line. The claimed

method which asserts a control line amounts to out-of-band signaling whereas the start-of-frame bit in a SONET signal is known as in-band signaling. The two are quite different and are not interchangeable in the context of the claimed invention. The passages in Wynn cited by the Examiner do not teach or suggest out-of-band signaling; they merely recite the SONET standard use of overhead bits.

Claims 13 and 14 depend from claim 10 and the remarks made above regarding claim 10 apply to these claims as well. Claim 13 requires "asserting a second control line at the first slot of the repeating bus frame". In rejecting claim 13, the Examiner refers to the start-of-packet bit taught by Wynn. Again, the Examiner is confusing in-band with the claimed assertion of a control line which amounts to out-of-band signaling. In addition, the Examiner is assuming that the start-of-packet bit corresponds in time with the first slot of the repeating frame in Wynn. Of course this is impossible because the SONET signal is bit serial and the first slots of the SONET frame are specified by the SONET standard. Therefore the start-of-packet bit must occur long after the first slot.

Claim 14 requires "asserting a second control line when a slot of the repeating bus frame includes a framing signal of an asynchronous data stream." In rejecting claim 14, the Examiner refers to the end-of-frame bit or parity bit or "output control which generates a formatter frame signal for establishing frame relationships..." Again, the Examiner confuses in-band signaling with the claimed assertion of a control line. In addition, he confuses an indication that a slot contains a framing signal with the framing signal itself; i.e. the Examiner confuses the indicator with the thing indicated.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,

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